REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated December 19, 2002.

Claims 1-12 are under consideration in this application. Claims 1 and 5 are being amended, as set forth above and in the attached marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention. Claims 9-12 are being added to recite other embodiments described in the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Prior Art Rejections

Claims 1-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over US Pat. No. 5,091,784 to Someya et al. (hereinafter "Someya"). This rejection has been carefully considered, but is most respectfully traversed.

The liquid crystal display device of the invention (Embodiment 1 in Fig. 2 and Embodiment 2 in Fig. 23), as now recited in claim 1, having a liquid crystal display panel 100, a plurality of cascade-connected liquid crystal drive circuits 130, 140 for sequentially transferring a signal (Fig. 1; page 1, third line to the bottom; ""the display data and clock signal as sent out of the timing controller will be delivered and passed between respective drain drivers in a one-by-one manner," page 3, lines 17-19), and a plurality of signal lines (Fig. 1, not numbered) formed over an edge portion of the liquid crystal display panel for transmitting a signal between any two of the drive circuits. Each of the drive circuits comprises: an image input terminal connected with one of the signal lines to receive an image signal being input thereto; a clock input terminal connected with another one of the signal lines to receive an external clock signal being input thereto; a clock compensation circuit 200 (e.g. Fig. 3, page 17) for generating

an internal clock based on the external clock signal by compensating for a duty ratio deviation from the external clock signal (page 3, last paragraph; page 4, lines 20-23; page 50, 4th paragraph), said internal clock signal swinging from a first voltage to a second voltage lower than the first voltage; a data storage circuit for storing therein the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal; a data bus for transmitting the image signal from the data storage circuit; and a voltage select circuit for selecting from the image signal on the data bus a voltage used to drive the liquid crystal display panel and then outputting the voltage selected.

The duty ratio deviation from the clock signal is caused by at least one of an internal characteristic of the respective drive circuit, such as the threshold voltage (Vth) of each MOS transistor in a CMOS inverter circuit, a factor on the signal lines, or repeated signal transferring events (page 5, last paragraph to page 6, first paragraph). Preferably, the internal clock signal generated by the clock compensation circuit has a duty ratio of 50% ("Output Clock Signal" in Figs. 4, 9; page 18, lines 21-24; "Clock Signal (inverted)" in Fig. 26).

As the clock signal duty ratio variation increases via the increase of drive circuit stages, it will finally become impossible to accept any display data at the later driver circuits. The present invention avoid the problem by compensating the duty ratio of each output clock signal fo the respective drive circuit.

The invention (Embodiment 3 in Figs. 24-25), as now recited in claim 5, is also directed to a liquid crystal display device having a liquid crystal display element 52, a plurality of cascade-connected liquid crystal drive circuits, and a plurality of signal lines formed over an edge portion of the liquid crystal display panel for transmitting a signal between any two of the drive circuits. Each of the liquid crystal drive circuits comprises: a data input terminal connected with one of the signal lines to receive an image signal being input thereto; a clock compensation circuit for inputting an external clock and outputting an internal clock, the internal clock having a first period for outputting a first voltage and a second period for outputting a second voltage; a data latch circuit for taking thereto the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock; a data bus for transmitting the image signal from the data latch circuit; a voltage output circuit for outputting a voltage selected from the image signal on

the data bus to the liquid crystal display element; and a data output circuit for outputting the image signal on the data bus to a subsequent liquid crystal drive circuit. In particular, the clock compensation circuit corrects a duty ratio deviation from the external clock signal.

Applicants respectfully contend that neither Someya nor any other cited prior art reference teaches or suggests "a plurality of cascade-connected liquid crystal drive circuits for sequentially transferring a signal connected by a plurality of signal lines, each drive circuit having a clock compensation circuit for generating an internal(output) clock based on the external(output) clock signal by compensating for a duty ratio deviation from the external/input clock signal caused by an internal characteristic of the respective drive circuit and/or a factor on the signal lines" as the invention. The plurality of signal lines are formed over an edge portion of the liquid crystal display panel, and the image signal is stored each time a change of the internal clock signal (from a second voltage to a first voltage or vise verse) occurs.

In contrast, the clock generator 8 in Fig. 2 of Someya is located inside a ***control circuit*** 7 (rather than a ***drive circuit***). Someya performs double line sequential scanning on a display apparatus which displays, for example, a television signal and a character and graphics signal, to solve the problem of sticking or ghosting of the character and graphic images (Abstract). The clock generator 8 of Someya outputs different clock signals ("various clock signals" col. 6, line 67, i.e., **MANY** clock signals). On the other hand, each of the clock compensation circuit 200 in its respective drive circuit only generates **ONE** internal (output) clock signal based on the external (input) clock signal. Someya simply does not concern about any duty ratio deviation from an input clock signal caused by an internal characteristic of the respective drive circuit or a factor on the signal lines between the cascade-connected drive circuits. Someya does not teach (1) forming a plurality of signal lines which connect the drive circuits and are formed over an edge portion of the liquid crystal display panel; or (2) storing the image signal each time a change of the compensated/corrected internal clock signal (from a second voltage to a first voltage or vise verse) occurs.

Contrary to the Examiner's allegation that one skilled in the art would be motivated to correct the various internal/output clock signals in Someya based upon the external/input clock signal, Applicants respectfully contend that one skilled in the art can't derive the reason(s) or method(s) for such a correction as alleged based upon the cited paragraphs or any portions of Someya. The Examiner's reliance upon the "common

knowledge and common sense" of one skilled in the art for any motivation for compensating/correcting the clock signals in Someya does not fulfill the agency's obligation to cite references to support its conclusions. Instead, the Examiner must provide the specific teaching of the correction on the record, i.e., positive recitation in written text, to allow accountability.

> *To establish a prima facie case of obviousness, the Board must, inter alia, show "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved." Kotzab, 217 F.3d at 1370, 55 USPQ2d at 1317. .... Recently, in In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), we held that the Board's reliance on "common knowledge and common sense" did not fulfill the agency's obligation to cite references to support its conclusions. Id. at 1344, 61 USPQ2d at 1434. Instead, the Board must document its reasoning on the record to allow accountability. Id. at 1345, 61 USPQ2d at 1435.*
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> See In re Thrift, 298 F.3d 1357.

Such an obligation to provide specific teaching(s) also applies to other existing or future obviousness rejections.

Even if, arguendo, a person of ordinary skill were motivated to combine the teachings in Someya as specified by the Examiner, such combined teachings would still fall short in fully meeting the Applicants' claimed invention as set forth in claims 1 and 5 since, as discussed, there are no teachings of "a plurality of cascade-connected liquid crystal drive circuits for sequentially transferring a signal connected by a plurality of signal lines, each drive circuit having a clock compensation circuit for generating an internal(output) clock based on the external(output) clock signal by compensating for a duty ratio deviation from the external/input clock signal caused by an internal characteristic of the respective drive circuit and/or a factor on the signal lines" in Someya.

Applicants contend that neither Someya nor other cited references teaches or discloses

each and every feature of the present invention as disclosed in at least independent claims 1 and 5. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

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Marked-up Version of Amended Claims

1. A liquid crystal display device having a liquid crystal display panel, a plurality of cascade-connected liquid crystal drive circuits for sequentially transferring a signal, and a plurality of signal lines formed over an edge portion of the liquid crystal display panel for transmitting a signal between any two of the drive circuits, wherein each of the liquid crystal drive circuits comprises:

an image input terminal connected with one of the signal lines to receive an image signal being input thereto;

a clock input terminal connected with another one of the signal lines to receive an external clock signal being input thereto;

a clock compensation circuit for generating an internal clock based on the external clock signal [, the] by compensating for a duty ratio deviation from the external clock signal, said internal clock signal swinging from a first voltage to a second voltage lower than the first voltage;

a data storage circuit for storing therein [an] the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal;

a data bus [causing] for transmitting the image signal [to be output] from the data storage circuit; and

a voltage select circuit for selecting from the image signal [of] on the data bus a voltage used to drive the liquid crystal display panel and then outputting the voltage selected.

5. A liquid crystal display device having a liquid crystal display element, [and] a plurality of cascade-connected liquid crystal drive circuits, and a plurality of signal lines formed over an edge portion of the liquid crystal display panel for transmitting a signal between any two of the drive circuits, wherein each of the liquid crystal drive circuits comprises:

a data input terminal connected with one of the signal lines to receive an image signal being input thereto;

a clock compensation circuit for inputting an external clock and outputting an internal clock, the internal clock having a first period for [permitting] outputting [of] a first voltage and a second period for outputting [of] a second voltage;

a data latch circuit for taking thereto [an] the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock;

a data bus for transmitting[output of] the image signal from the data latch circuit;

a voltage output circuit for outputting a voltage selected from the image signal on the data bus to the liquid crystal display element; and

a data output circuit for outputting the image signal on the data bus to a subsequent [next stage of] liquid crystal drive circuit[; and], wherein

the clock compensation [formation] circuit [being operable to] corrects a duty ratio deviation from the external clock signal[the internal clock based on the external clock].